Electronic Version
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Description

A Dual-Loop PLL with DAC offset for Frequency Shift While Maintaining Input Tracking

BACKGROUND OF INVENTION

[0001] This invention relates to phase-locked loops (PLL's), and more particularly to dual-loop PLLs with frequency shift.

[0002] Many electronic systems are synchronous or clocked. These systems may rely on accurate clocks to synchronize the timing of operations and data transfers. A crystal oscillator can be used to generate a clock at a base frequency, which is then divided or multiplied to create one ore more clocks with desired frequencies. External clock can be received and likewise divided or multiplied to produce internal clocks.

[0003] Clocks are typically generated from oscillator outputs using phase-locked loops (PLL's). PLLs are one of the most widely use building blocks in digital systems today. Figure 1 illustrates a typical PLL. Phase detector 10 receives a

reference-clock input from an external oscillator or clock source. The phase and frequency of the reference clock is compared to the phase and frequency of a feedback clock generated by voltage-controlled oscillator (VCO) 14. The feedback clock can be the output clock generated by the PLL, or a divided-down derivative of the output clock from VCO 14 such as produced by feedback counter 16.

[0004] Phase detector 10 outputs up and down signals UP, DN when the phase or frequency of one input does not match the phase or frequency of the other input. These up and down signals cause charge pump 12 to add or remove charge from filter capacitor 20, which integrates the charge. As charge is added or removed through resistor 21 from filter capacitor 20, the voltage input to VCO 14 is increased or decreased. VCO 14 responds by increasing or decreasing the frequency of the output clock. The feedback clock to phase detector 10 is likewise changed by VCO 14.

[0005] As charge pump 12 adds or removes charge from filter capacitor 20, altering control voltage V_{CTL} input to VCO 14, the phase and frequency of the feedback clock are adjusted until the reference clock is matched. Then phase detector 10 stops generating up and down signals to

charge pump 12, until charge leaks off filter capacitor 20 or the reference clock changes.

[0006] Pulses of short duration are often used for up and down signals UP, DN. For example, phase detector 10 can be a pair of simple flip-flops. One flip-flop outputs the UP pulse when clocked by the reference-clock input. The UP pulse ends when cleared by the feedback-clock input. The other flip-flop generates the DN pulse when clocked by the feedback-clock input. The DN pulse ends when cleared by the reference-clock input. As the phases match more closely, the duration of the pulses shorten.

[0007] Often both up and down signals are pulsed simultaneously when little or no phase adjustment is needed. Charge pump 12 should supply either no charge or equal up and down charges to filter capacitor 20 so that a net zero charge is supplied when the duration of simultaneous UP and DN pulses are identical.

[0008] Sometimes the frequency of the reference clock shifts over time, either intentionally or unintentionally. Intention frequency shifts may occur as line conditions change, such as when a communications channel experiences better conditions and can handle a higher bit rate for a period of time.

[0009] Since clocks are intended to be stable, such frequency shifts may be difficult to track. The PLL may lose sync or otherwise produce erroneous results. The net charge added to filter capacitor 20 may not exactly compensate for the frequency shift, resulting in a phase error. VCO 14 may responds by slightly changing the phase and frequency of the feedback clock so that it no longer exactly matches the reference clock.

[0010] Figure 2 is a timing diagram of UP and DOWN inputs to a charge pump and the resulting control voltage to the VCO when the reference frequency is shifted. When the frequency of the input reference clock is shifted upward, a leading phase difference is detected by the phase detector, and an UP pulse is generated. The charge pump responds to the UP pulse by pumping positive charge to the filter capacitor, increasing the control voltage V_{CTL} to the VCO. The amount of charge pumped to the filter capacitor depends on the duration of the UP pulse. Once the frequency shift ends, the UP pulse ends, and the control voltage remains stable. Down pulses DN may also be activated during the shift when the frequency shift is relatively slow.

[0011] Ideally, the net current of the UP and DN pulses should

match the frequency shift. The net charge added to the control voltage should exactly match the new frequency. This net charge added by the charge pump shifts the frequency of the VCO.

[0012] What is desired is a PLL that can smoothly respond to a shift in the input frequency. A PLL that can have a frequency offset is desirable. A frequency-shifting PLL is desirable.

Brief Description of Drawings

[0013] Figure 1 illustrates a typical PLL.

[0014] Figure 2 is a timing diagram of UP and DOWN inputs to a charge pump and the resulting control voltage to the VCO when the reference frequency is shifted.

[0015] Figure 3 is a block diagram of a single-loop PLL with a DAC for frequency shifting.

[0016] Figure 4 shows a dual-loop PLL with frequency offset controlled by a DAC.

Detailed Description

[0017] The present invention relates to an improvement in phase-locked loops (PLL's). The following description is presented to enable one of ordinary skill in the art to make and use the invention as provided in the context of

a particular application and its requirements. Various modifications to the preferred embodiment will be apparent to those with skill in the art, and the general principles defined herein may be applied to other embodiments. Therefore, the present invention is not intended to be limited to the particular embodiments shown and described, but is to be accorded the widest scope consistent with the principles and novel features herein disclosed.

[0018] Figure 3 is a block diagram of a single-loop PLL with a DAC for frequency shifting. Phase detector 32 compares the phase of reference clock REF_CLK to the output clock OUT_CLK (or another feedback clock). Phase differences activate charge pump 34 to charge or discharge filter capacitor 38. As the voltage on filter capacitor 38 changes, op amp 50 transmits these voltage changes on node N1 to node N2, the input to voltage-controlled oscillator VCO 36, adjusting the frequency of output clock OUT_CLK.

[0019] The output from digital-to-analog converter DAC 52 is normally turned off, so no current flows from DAC 52 through resistor 54. Then op amp 50 replicates its non-inverting input from node N1, the voltage of filter capacitor 38, to its output, node N2.

[0020] When a frequency shift is desired, switch 62 opens to dis-

connect charge pump 34 from filter capacitor 38. Node N1 is isolated and remains at a constant voltage except for leakage over a very long period of time. DAC 52 turns on and drives a current through resistor 54. The amount of the current depends on the digital value input to DAC 52. The current through resistor 54 produces a voltage difference between the output and inverting input of op amp 50.

[0021] The voltage offset across resistor 54 increases or decreases the voltage of node N2, the VCO input, relative to the filter voltage on node N1, depending on whether the current is positive or negative from DAC 52. Thus the frequency generated by VCO 36 can be increased or decreased by DAC 52.

[0022] Once the desired frequency has been reached by VCO 36, switch 62 can be opened and phase detector 32 causes the shifted-frequency output clock OUT_CLK to stop tracking the reference clock REF_CLK with the added offset from resistor 54. DAC 52 can be kept on to maintain the offset on resistor 54.

[0023] Figure 4 shows a dual-loop PLL with frequency offset controlled by a DAC. A second tracking loop of phase detector 42, charge pump 44, filter capacitor 48 on node N3 to

VCO 46 cause a second clock L2_CLK to track reference clock REF_CLK. This second loop is isolated from the primary loop by switch 64. When DAC 52 initiates a frequency shift, switch 63 opens to isolate OUT_CLK from phase detector 32. Switch 64 closes, allowing the second loop to continue tracking the input reference clock as the frequency shift occurs.

[0024] In the primary loop, phase detector 32 compares the phase of reference clock REF_CLK to the output clock L2_CLK of the secondary loop (or another feedback clock such as from a divider). Phase differences activate charge pump 34 to charge or discharge filter capacitor 38. As the voltage on filter capacitor 38 changes, op amp 50 transmits these voltage changes on node N1 to node N2, the input to voltage-controlled oscillator VCO 36, adjusting the frequency of output clock OUT_CLK.

[0025] The output from digital-to-analog converter DAC 52 is normally turned off, so no current flows from DAC 52 through resistor 54. Then op amp 50 replicates its non-inverting input from node N1, the voltage of filter capacitor 38, to its output, node N2.

[0026] When a frequency shift is desired, switch 63 opens to disconnect OUT_CLK from phase detector 32. Also switch 64

closes to connect the second loop and the primary loop. DAC 52 turns on and drives a current through resistor 54. The amount of the current depends on the digital value input to DAC 52.

[0027] The current through resistor 54 produces a voltage difference between the output and inverting input of op amp 50. The voltage offset across resistor 54 increases or decreases the voltage of node N2, the VCO input, relative to the filter voltage on node N1, depending on whether the current is positive or negative from DAC 52. Thus the frequency generated by VCO 36 can be increased or decreased by DAC 52.

[0028] Any tracking changes due to changes in reference clock REF_CLK that occurred while DAC 52 was shifting the frequency are captured by the second loop as the second loop's output L2_CLK follows changes of input REF_CLK. At the same time, phase detector 32 detects any phase differences between REF_CLK and L2_CLK and feeds an error signal into node N1 of the primary loop. Any such voltage change is thus coupled to node N1 of the primary loop when switch 64 is closed.

[0029] Phase detector 32 in the primary loop causes the shifted-frequency output clock OUT_CLK to continue tracking the

reference clock REF_CLK with the added offset from resistor 54. Phase detector 32 keeps track of errors between REF_CLK and L2_CLK for every cycle.

[0030] The voltage offset across resistor 54 is maintained by op amp 50, causing nodes N1 and N2 to have different voltages, and causing OUT_CLK and REF_CLK to have differing frequencies with a difference in frequency determined by the voltage offset. As reference clock REF_CLK changes in phase or frequency, these input-clock changes continue to adjust the output clock, but the output clock continues to be offset in frequency by the amount determined by the voltage offset across resistor 54.

[0031] ALTERNATE EMBODIMENTS

[0032] Several other embodiments are contemplated by the inventor. For example the charge pump, phase comparator, VCO, switches, and DAC can be implemented by a variety of circuits and technologies. Other filters can be substituted for capacitors 38, 48, such as filters with inductances, series resistances, or parallel legs. Additional PLL loops can be added, and more complex circuits can be substituted. Feedback counters may added or simply divide by one rather than a larger divisor. Other rectifier circuits could be used in place of the diode. Coupling of

nodes can be through capacitors or resistors. The DAC can be implemented in a variety of technologies and circuits and may include current-sources of various steps, switched-capacitor, and other techniques.

[0033] The current from the DAC can be slowly ramped or stepped by sequencing the DAC input through intermediate digital values rather than initially applying the final value. The exact frequency offset can be determined empirically or by simulation, and may be adjusted by trimming the DAC or resistor value. Trimming may be done by adjusting the digital value used for the desired frequency shift.

[0034] The switch after the VCO may be a disable logic control input to the phase detector rather than a discrete switch. Switches may also be implemented as transmission gates of pass transistors. The op amp can be a standard operational amplifier implemented with any of a variety of circuits.

[0035] The abstract of the disclosure is provided to comply with the rules requiring an abstract, which will allow a searcher to quickly ascertain the subject matter of the technical disclosure of any patent issued from this disclosure. It is submitted with the understanding that it will not be used

to interpret or limit the scope or meaning of the claims. 37 C.F.R. § 1.72(b). Any advantages and benefits described may not apply to all embodiments of the invention. When the word "means" is recited in a claim element, Applicant intends for the claim element to fall under 35 USC § 112, paragraph 6. Often a label of one or more words precedes the word "means". The word or words preceding the word "means" is a label intended to ease referencing of claims elements and is not intended to convey a structural limitation. Such means-plus-function claims are intended to cover not only the structures described herein for performing the function and their structural equivalents, but also equivalent structures. For example, although a nail and a screw have different structures, they are equivalent structures since they both perform the function of fastening. Claims that do not use the word means are not intended to fall under 35 USC § 112, paragraph 6. Signals are typically electronic signals, but may be optical signals such as can be carried over a fiber optic line.

[0036] The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or

to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.